



Overview

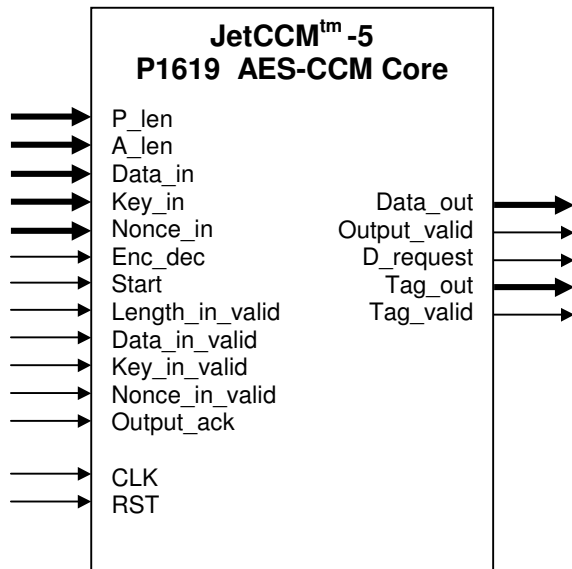
The tape storage security specified by IEEE P1619.1 utilizes the NIST standard AES in CCM mode for both encryption and message authentication. The CCM mode uses 256-bit key AES and combines the counter mode of encryption with the CBC-MAC mode of authentication.

The **JetCCMtm-5** core is optimized for IEEE P1619.1 applications. The core includes our fully verified JetAEStm cryptographic core and supports encryption, decryption, authentication, and verification functionalities. Its design is fully synchronous for portability. The core is available for licensing in both source and netlist form.

Application

IEEE P1619.1 tape storage applications

Features
➤ Fully compliant with IEEE P1619.1 AES-CCM mode
➤ High throughput > 2 Gbps
➤ Simple interface
➤ Fully synchronous design
➤ Flow-through design
➤ Combine both AES-CCM encryption-authentication and decryption-verification
➤ Support 256-bit key size based on IEEE P1619.1 requirements
➤ On-the-fly hardware key expansion
➤ Key expansion can also be performed in software to reduced the gate count
➤ Core is available as a synthesizable Verilog source code, or as a netlist
➤ Self-checking test bench



General Description

Advanced Encryption Standard (AES), also known as Rijndael, is a block cipher adopted as an encryption standard by NIST to replace DES. DES is now considered to be insecure for many applications.

CCM mode (Counter with CBC-MAC) is a mode of operation for use with block cipher such as AES. CCM mode combines the counter mode of encryption with the CBC-MAC mode of authentication.

IEEE P1619.1 specifies an architecture for protection of data in variable-length block storage media such as tape cartridge. It utilizes the NIST standard AES in CCM mode with 256-bit key size for privacy and integrity of data stored on tape.

JetCCMTM-5 core is an AES-CCM core optimized for IEEE P1619.1 tape storage applications and includes the fully verified JetAESTM cryptographic module. The core supports encryption, authentication, decryption, and verification functionalities. It implements a 128-bit wide data path and 128-bit wide data interfaces.

JetCCMTM-5 core supports 256-bit key size based on IEEE P1619.1 requirements. The core is implemented for flow-through operation. Its design is fully synchronous for portability.

The key expansion logic inside the core works as a standalone block which can generate the AES roundkeys on-the-fly. If the input key does not change frequently, then the roundkeys can be pre-expanded and stored in memory by the Key Expansion Logic. Alternatively, the roundkeys can also be generated and stored in memory by an embedded processor. Thus, these options can further reduce gate count.

Core I/O

The core I/O signals of the JetCCMTM-5 core with hardware on-the-fly key expansion for the 256-bit key size are described in the table below.

Signal	I/O	Width	Description
CLK	Input	1	Master clock
RST	Input	1	Master reset; 1 = reset
P_len	Input	32	Length of plain text in bytes
A_len	Input	64	Length of AAD in bytes
Data_in	Input	128	Data input (AAD and plaintext)
Key_in	Input	256	Key input
Nonce_in	Input	103	Nonce input
Enc_dec	Input	1	0 = Encryption; 1= Decryption

Start	Input	1	Start processing
Length_in_valid	Input	1	Length in valid signal
Data_in_valid	Input	1	Data_in valid signal
Key_in_valid	Input	1	Key_in valid signal
Nonce_in_valid	Input	1	Nonce_in valid signal
Output_ack	Input	1	Output acknowledgement
Data_out	Output	128	Data output
Output_valid	Output	1	Output data valid
D_request	Output	1	Data input request
Tag_out	Ouput	128	Tag out
Tag_valid	Ouput	1	Tag valid

Implementation Results

Example ASIC implementation statistics for the JetCCMtm-5 core are shown below

Technology	Gate Count
TSMC 0.18 μ m	74638

Example implementation statistics on FPGAs for the JetCCMtm-5 core are shown below

Xilinx Family	Device	Slices	BRAM	CLK	I/O	Fmax (MHz)
Spartan-3E tm	XC3S250E-4	1585	10	1	851	89
Spartan-3 tm	XC3S200-5	1619	10	1	851	112
Virtex-II Pro tm	XC2VP2-7	1572	10	1	851	195
Virtex-4 tm	XC4VLX25-11	1609	10	1	851	249
Virtex-5 tm	XC5VLX30	584	20	1	851	294

Support

Sixty days of phone and email technical support are included. Additional maintenance and support options are available.

Verification

The JetCCMtm-5 core has been thoroughly simulated and verified on Xilinx FPGA hardware using the NIST test vectors and additional software-generated test vectors.

Deliverables

The core is available in soft IP form, either as a Netlist or HDL Source. The deliverables include:

- For **Netlist Licenses** : Target specific net list
- For **HDL Licenses** : Fully synthesizable RTL Verilog source
- Self-checking test bench
- Simulation script, test vectors and expected results
- User documentation

Export Permits

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or

www.jetsmt.com

Jetstream Media Technologies
800 W. 5th Ave.
Naperville, IL 60563 U.S.A.
Tel: 1 (630)-301-4778
Email: sales@jetsmt.com